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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PRENTY, MARK V	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 01/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,477	YAMAZAKI, SHUNPEI	
	Examiner	Art Unit	
	MARK V PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2003 and 05 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-30,33-35,38-45,48-50 and 53* is/are rejected.

7)☒ Claim(s) *31,32,36,37,46,47,51 and 52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/192,745.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *January 5, 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This Office Action is in response to the papers filed on October 27, 2003 and January 5, 2004.

Claims 26, 27, 31, 32, 36, 37, 41, 42, 46, 47, 51 and 52 are objected to because "the second impurity regions" lack antecedent basis in independent claims 24, 29, 34, 39, 44 and 49, which recite "a second impurity region." Correction is required.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 24 and 39 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of parent United

States Patent 6,686,623. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 24 and 39 are broader than the parent patent's claim 2.

Claims 26 and 41 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 26 of parent United States Patent 6,686,623. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 26 and 41 are broader than the parent patent's claim 26.

Claims 27 and 42 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 27 of parent United States Patent 6,686,623. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 27 and 42 are broader than the parent patent's claim 27.

Claims 24, 25, 29, 30, 34, 35, 39, 40, 44, 45, 49 and 50 are rejected under 35 U.S.C. 102(e) as being anticipated by Liu et al. (United States Patent 5,814,854 – hereafter Liu – cited in the Information Disclosure Statement filed on January 5, 2004).

With respect to independent claim 24, Liu discloses a semiconductor device (see the entire patent, including the Figs. 5D-5E disclosure) comprising: a semiconductor film (see the Fig. 5E disclosure); a pair of first impurity regions 118 and 116 being formed in the semiconductor film (see the Fig. 5D disclosure); an active region formed between the pair of first impurity regions in the semiconductor film; a second impurity region 112 formed partly in said [crystal] semiconductor film between the pair of impurity

regions; a floating gate 110 formed over and insulated from the active region; and a control gate 108 formed over and insulated from the floating gate, wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the second impurity region.

Claim 24 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Liu.

With respect to dependent claim 25, Liu's second impurity region 112 has a striped shape.

Claim 25 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Liu.

With respect to independent claim 29, Liu discloses a semiconductor device (see the entire patent, including the Figs. 5D-5E disclosure) comprising: a NOR type circuit (see column 4, lines 13-16) having a plurality of memory transistors, the memory transistor comprising: a semiconductor film (see the Fig. 5E disclosure); a pair of first impurity regions 118 and 116 being formed in the semiconductor film (see the Fig. 5D disclosure); an active region formed between the pair of first impurity regions in the semiconductor film; a second impurity region 112 formed partly in said semiconductor film between the pair of impurity regions; a floating gate 110 formed over and insulated from the active region; and a control gate 108 formed over and insulated from the floating gate, wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the second impurity region.

Claim 29 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Liu.

With respect to dependent claim 30, Liu's second impurity region 112 has a striped shape.

Claim 30 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Liu.

With respect to independent claim 34, Liu discloses a semiconductor device (see the entire patent, including the Figs. 5D-5E disclosure) comprising: a NAND type circuit (see column 4, lines 13-16) having a plurality of one memory transistor, the memory transistor comprising: a semiconductor film (see the Fig. 5E disclosure); a pair of first impurity regions 118 and 116 being formed in the semiconductor film (see the Fig. 5D disclosure); an active region formed between the pair of first impurity regions in the semiconductor film; a second impurity region 112 formed partly in said [crystal] semiconductor film between the pair of impurity regions; a floating gate 110 formed over and insulated from the active region; and a control gate 108 formed over and insulated from the floating gate, wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the second impurity region.

Claim 34 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Liu.

With respect to dependent claim 35, Liu's second impurity region 112 has a striped shape.

Claim 35 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Liu.

With respect to independent claim 39, Liu discloses a semiconductor device (see the entire patent, including the Figs. 5D-5E disclosure) comprising: a substrate having an insulating surface; a semiconductor film provided over the substrate (see the Fig. 5E disclosure); a pair of first impurity regions 118 and 116 being formed in the semiconductor (see the Fig. 5D disclosure); an active region formed between the pair of first impurity regions in the semiconductor film; a second impurity region 112 formed

partly in said [crystal] semiconductor film between the pair of impurity regions; a floating gate 110 formed over and insulated from the active region; and a control gate 108 formed over and insulated from the floating gate, wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the second impurity region.

Claim 39 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Liu.

With respect to dependent claim 40, Liu's second impurity region 112 has a striped shape.

Claim 40 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Liu.

With respect to independent claim 44, Liu discloses a semiconductor device (see the entire patent, including the Figs. 5D-5E disclosure) comprising: a NOR type circuit (see column 4, lines 13-16) having a plurality of memory transistors, the memory transistor comprising: a substrate having an insulating surface; a semiconductor film provided over the substrate (see the Fig. 5E disclosure); a pair of first impurity regions 118 and 116 being formed in the semiconductor film (see the Fig. 5D disclosure); an active region formed between the pair of first impurity regions in the semiconductor film; a second impurity region 112 formed partly in said semiconductor film between the pair of impurity regions; a floating gate 110 formed over and insulated from the active region; and a control gate 108 formed over and insulated from the floating gate, wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the second impurity region.

Claim 44 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Liu.

With respect to dependent claim 45, Liu's second impurity region 112 has a striped shape.

Claim 45 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Liu.

With respect to independent claim 49, Liu discloses a semiconductor device (see the entire patent, including the Figs. 5D-5E disclosure) comprising: a NAND type circuit (see column 4, lines 13-16) having a plurality of one memory transistor, the memory transistor comprising: a substrate having an insulating surface; a semiconductor film provided over the substrate (see the Fig. 5E disclosure); a pair of first impurity regions 118 and 116 being formed in the semiconductor film (see the Fig. 5D disclosure); an active region formed between the pair of first impurity regions in the semiconductor film; a second impurity region 112 formed partly in said [crystal] semiconductor film between the pair of impurity regions; a floating gate 110 formed over and insulated from the active region; and a control gate 108 formed over and insulated from the floating gate, wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the second impurity region.

Claim 49 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Liu.

With respect to dependent claim 50, Liu's second impurity region 112 has a striped shape.

Claim 50 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Liu.

Claims 28, 33, 38, 43, 48 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (United States Patent 5,814,854 – hereafter Liu – cited in the Information Disclosure Statement filed on January 5, 2004) together with Yamazaki

et al. (United States Patent 6,127,702 – hereafter Yamazaki – cited in the Information Disclosure Statement filed on January 5, 2004).

Claims 28, 33, 38, 43, 48 and 53 depend on independent claims 24, 29, 34, 39, 44 and 49, respectively, which are rejected under 35 U.S.C. 102(e) as being anticipated by Liu (see above). The above explanation of the rejection of independent claims 24, 29, 34, 39, 44 and 49 under 35 U.S.C. 102(e) as being anticipated by Liu is hereby incorporated by reference into this rejection of dependent claims 24, 29, 34, 39, 44 and 49 under 35 U.S.C. 103(a) as being unpatentable over Liu together with Yamazaki.

The difference, therefore, between dependent claims 28/33/38/43/48/53 and Liu is the former's semiconductor device is used in any one of various electronic devices.

Yamazaki teaches that semiconductor devices are conventionally used in various electronic devices (see column 26, lines 53, through column 27, line 36).

It would have been obvious to one skilled in the art to use Liu's semiconductor device in any one of the recited electronic devices because Yamazaki teaches that semiconductor devices are conventionally used in such electronic devices.

Claims 28, 33, 38, 43, 48 and 53 are thus rejected under 35 U.S.C. 103(a) as being unpatentable over Liu together with Yamazaki.

PCT Publication WO 97/02605 (Ranaweera et al.) is relevant to this application.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

Mark Prenty

Mark V. Prenty
Primary Examiner